Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the above-identified application:

Listing of Claims:

1. (Currently Amended) A latch circuit having [[an]] a total current and at least one output, the output having a first state and a second state, the output being controllable by a first trigger signal and a second trigger signal, the latch circuit comprising:

a SET circuit;

a RESET circuit; and

wherein at least one of the conditions from the group consisting of the following is true: 1) at the first state, [[a]] the total current is conducted by the SET circuit, ~~[such that]~~ wherein the SET circuit ~~is maintained such that a first switching threshold is obtainable by using the first trigger signal~~ switches when the first trigger signal is applied to the SET circuit, and wherein the first trigger signal is less than 0.7 volts, and 2) at the second state, the total current is conducted by the RESET circuit, wherein the RESET circuit ~~is maintained such that a second switching threshold is obtainable by using the second trigger signal and 3) a combination of 1 and 2, wherein the latch circuit forms a switching portion of an oscillator circuit~~ switches when the second trigger signal is applied to the RESET circuit, and wherein the second trigger signal is less than 0.7 volts.

2. (Currently Amended) [[A]] The latch circuit of claim 1 ~~having an output, the output having a first state and a second state, the output being controllable by a first trigger signal and a second trigger signal, the latch circuit comprising:~~

~~a SET circuit;~~

~~a RESET circuit; and~~

~~wherein one condition from the group consisting of the following is true: 1) at the first state, a current is conducted by the SET circuit, wherein the SET circuit is maintained such that a first switching threshold is obtainable by using the first trigger signal 2) at the second state, the current is conducted by the RESET circuit wherein the RESET circuit is maintained such that a second switching threshold is obtainable by using the second trigger signal and 3) a combination of 1 and 2,~~ wherein the latch circuit forms a switching portion of a temperature-compensated oscillator circuit.

3. (Original) The latch circuit of claim 2, the temperature-compensated oscillator circuit further comprising level-shifting circuitry.

4. (Currently Amended) A latch circuit having a total current and at least one output, the output having a first state and a second state, the output being controllable by a first trigger signal and a second trigger signal, the latch circuit comprising:

a first latch transistor;

a second latch transistor coupled to the first latch transistor;

a SET transistor coupled to the first latch transistor; and

a RESET transistor coupled to the second latch transistor wherein at least one of the conditions from the group consisting of the following is true: 1) at the first state, [[a]] the total current is conducted by the first latch transistor and the SET transistor, wherein the SET transistor ~~is biased such that a first threshold is obtainable by using the first trigger signal~~ switches when

the first trigger signal is applied to the SET transistor, and wherein the first trigger signal is less than the full Vbe voltage of the SET transistor, and 2) at the second state, the total current is conducted by the second latch transistor and the RESET transistor, wherein the RESET transistor ~~is biased such that a second threshold is obtainable by using the second trigger signal 3) a combination of 1) and 2), wherein the latch circuit forms a switching portion of an oscillator circuit~~ switches when the second trigger signal is applied to the RESET transistor, and wherein the second trigger signal is less than the full Vbe voltage of the RESET transistor.

5. (Currently Amended) A method of oscillating the output of an oscillator, the output having a first state and a second state, the oscillator including a latch, the latch including a first latch transistor, a second latch transistor, a SET transistor and a RESET transistor, the method comprising:

at the first state, conducting a ~~first~~ total current in the first latch transistor and the SET transistor such that the SET transistor is biased at a point close to a first threshold;

at the second state, conducting the ~~first~~ total current in the second latch transistor and the RESET transistor such that the RESET transistor is biased at a point close to a second threshold;

varying the output from the first state to the second state by ~~providing~~ a first trigger ~~current~~ signal to ~~raise the base of~~ switch the SET transistor ~~over a first threshold~~, wherein the first trigger signal is less than the full Vbe voltage of the SET transistor; and

varying the output from the second state to the first state by ~~providing~~ a second trigger ~~current~~ signal to ~~raise the base of~~ switch the RESET transistor

~~over a second threshold~~, wherein the second trigger signal is less than the full Vbe voltage of the RESET transistor.

6. (Original) The method of claim 5 further comprising temperature compensating the oscillator.

7. (New) An oscillator circuit comprising the latch circuit of claim 1, wherein the oscillator circuit further comprises an oscillator capacitor coupled to the SET circuit, such that, at the first state, the capacitor is substantially charged, and at the second state, the capacitor is substantially discharged.

8. (New) The oscillator circuit of claim 7 further comprising a second current for charging the capacitor.

9. (New) The oscillator circuit of claim 8, further comprising a current source for producing the second current.

10. (New) The oscillator circuit of claim 9, further comprising an oscillator transistor coupled between the current source and the RESET circuit.

11. (New) The oscillator circuit of claim 10, further comprising a source of electrical potential coupled to the base of the oscillator transistor.

12. (New) The oscillator circuit of claim 10, further comprising temperature compensating circuitry for compensating the oscillator transistor, such that the difference between an upper oscillator threshold of the capacitor and a lower oscillator threshold of the capacitor remains constant.

13. (New) The latch circuit of claim 1, wherein a de-bias circuit is coupled between the SET circuit and ground.

14. (New) The latch circuit of claim 1, wherein a de-bias circuit is coupled between the RESET circuit and ground.

15. (New) The latch circuit of claim 1, wherein the total current is provided by a plurality of current sources, and each of the plurality of current sources are coupled to a source of electrical potential.

16. (New) The latch circuit of claim 1, wherein the total current is provided by two substantially equivalent current sources, and the current sources are coupled to a source of electrical potential.

17. (New) The latch circuit of claim 1, wherein about one-half of the total current is provided by a first current source and about one-half of the total current is provided by a second current source, and the first and second current sources are coupled to a source of electrical potential.

18. (New) The latch circuit of claim 1, wherein the total current is about 200 microamperes.

19. (New) The latch circuit of claim 1, wherein, at the first state, the total current is substantially continuously conducted by the SET circuit.

20. (New) The latch circuit of claim 1, wherein, at the second state, the total current is substantially continuously conducted by the RESET circuit.

21. (New) The latch circuit of claim 1, wherein, when said first trigger signal is applied to said SET circuit, said RESET circuit switches ON.

22. (New) The latch circuit of claim 1, wherein, when said second trigger signal is applied to said RESET circuit, said SET circuit switches ON.

23. (New) The latch circuit of claim 1, wherein the first trigger signal is about 0.018 volts.

24. (New) The latch circuit of claim 1, wherein the second trigger signal is about 0.018 volts.

25. (New) The latch circuit of claim 4, wherein the first trigger signal is more than an order of magnitude less than the full Vbe voltage of the SET transistor.

26. (New) The latch circuit of claim 4, wherein the second trigger signal is more than an order of magnitude less than the full Vbe voltage of the RESET transistor.

27. (New) The latch circuit of claim 4, wherein the first trigger signal is about 0.018 volts.

28. (New) The latch circuit of claim 4, wherein the second trigger signal is about 0.018 volts.

29. (New) The latch circuit of claim 4, wherein, the first latch transistor and the second latch transistor are cross-coupled to one another.

30. (New) The latch circuit of claim 4, wherein, at the first state, the total current is divided between

the first latch transistor and the SET transistor at a pre-determined ratio.

31. (New) The latch circuit of claim 4, wherein, at the second state, the total current is divided between the second latch transistor and the RESET transistor at a pre-determined ratio.

32. (New) The latch circuit of claim 4, wherein the SET transistor and the first latch transistor are a first BJT transistor and a second BJT transistor, respectively.

33. (New) The latch transistor of claim 32, wherein the base and emitter of the first latch transistor are coupled to the base and emitter of the SET transistor, respectively.

34. (New) The latch circuit of claim 4, wherein a resistor is coupled between the base of the SET transistor and the base of the first latch transistor.

35. (New) The latch circuit of claim 4, wherein each of the first latch transistor, the second latch transistor, the SET transistor and the RESET transistor is an NPN transistor, and the total current is provided as a current source to the transistors.

36. (New) The latch circuit of claim 4, wherein each of the first latch transistor, the second latch transistor, the SET transistor and the RESET transistor is a PNP transistor, and the total current is provided as a current sink from the transistors.

37. (New) The latch circuit of claim 4, wherein the total current is provided by two substantially equivalent current sources, and the current sources are coupled to a source of electrical potential.

38. (New) The method of claim 5, wherein the first trigger signal is more than an order of magnitude less than the full Vbe voltage of the SET transistor.

39. (New) The method of claim 5, wherein the second trigger signal is more than an order of magnitude less than the full Vbe voltage of the RESET transistor.